Mentor Graphics USB 2.0 Reference Design for Home Networking Solutions

This leaflet describes a USB 2.0 Transfer System board, which provides a reference design for home networking applications that use the USB 2.0 Universal Serial Bus.

The board comprises a USB 2.0-compliant function controller, an 8051-compatible microcontroller and a DMA controller implemented in two Xilinx Spartan®-II FPGAs, together with a Kawasaki USB 2.0 transceiver. It provides an interface for high-speed data transfer between a PC and a SCSI disk drive.

The Mentor Graphics USB 2.0 Transfer System represents a complete solution for low cost, high performance data connection.

Key features

- Low-cost solution
- High speed operation, up to 480Mbits/sec
- *USB 2.0 function controller*
  - ❑ Mentor Graphics MUSBHSFC core
  - ❑ Complies with industry standards
  - ❑ 16-bit VCI interface to microcontroller
  - ❑ 16-bit UTMI interface to USB transceiver
  - ❑ 2 Bulk Endpoints with 1024byte synchronous FIFOs
  - ❑ Firmware included
- *8051 microcontroller*
  - ❑ Mentor Graphics M8051 E-Warp core
  - ❑ 2 clocks per cycle, running at 16 MHz
  - ❑ Complies with industry standards
  - ❑ 16-bit asynchronous interface to SCSI bus
  - ❑ 64K bytes external program memory (<10K used)
  - ❑ 64K bytes external data memory
  - ❑ On-Chip debug with JTAG interface
  - ❑ Source-level debug (in ‘C’)
- *FPGA Implementation*
  - ❑ Xilinx Spartan®-II FPGA
  - ❑ Two XC2S200-6PQ208 devices
  - ❑ Density up to 200,000 system gates
  - ❑ Block RAM up to 56K bit
  - ❑ Reprogrammable

USB 2.0 Transfer Architecture

PC with USB 2.0 Host, running Windows 2000

USB

Mentor Graphics USB 2.0 Transfer System Board

SCSI

SCSI Disk Drive

01/01 MB-40113.001-PO

System Overview

The figure below shows the board block diagram.

The principal constituents of the board are a USB 2.0 function controller and a 8051 microcontroller. These two devices are provided by reusable and configurable soft cores from the Mentor Graphics Inventra™ IP catalog, implemented in Xilinx Spartan®-II FPGAs. The USB 2.0 function controller is provided by the Inventra™ MUSBHSFC soft core; the 8051 microcontroller is provided by the Inventra™ M8051 E-Warp soft core.

One FPGA contains the MUSBHSFC core, together with the RAM needed to provide FIFOs for the function controller's endpoints. The MUSBHSFC is configured to support two Bulk endpoints in addition to the control Endpoint 0. The Endpoint FIFOs use eight of the memory blocks available within the FPGA.

The other FPGA contains the M8051 E-Warp core together with a DMA controller. The data and program memory for the microcontroller is provided by two external memory chips, one Flash and one SRAM, plus 4Kbytes of internal memory.

The other main component of the board is a USB 2.0 transceiver chip from Kawasaki, the KL5KUSB200, which provides the connection between the USB serial bus and the UTMI bus for both high-speed and full-speed operation.

The MUSBHSFC uses an internal 30 MHz clock and the data transfers are executed on 16-bit buses. The bus on the USB 2.0 transceiver side is UTMI compliant; the bus on the microcontroller side is VCI compliant.

USB Device Software

The software controlling the USB device implements Universal Serial Bus Mass Storage Class, Bulk-Only Transport (Specification Revision 1.0).

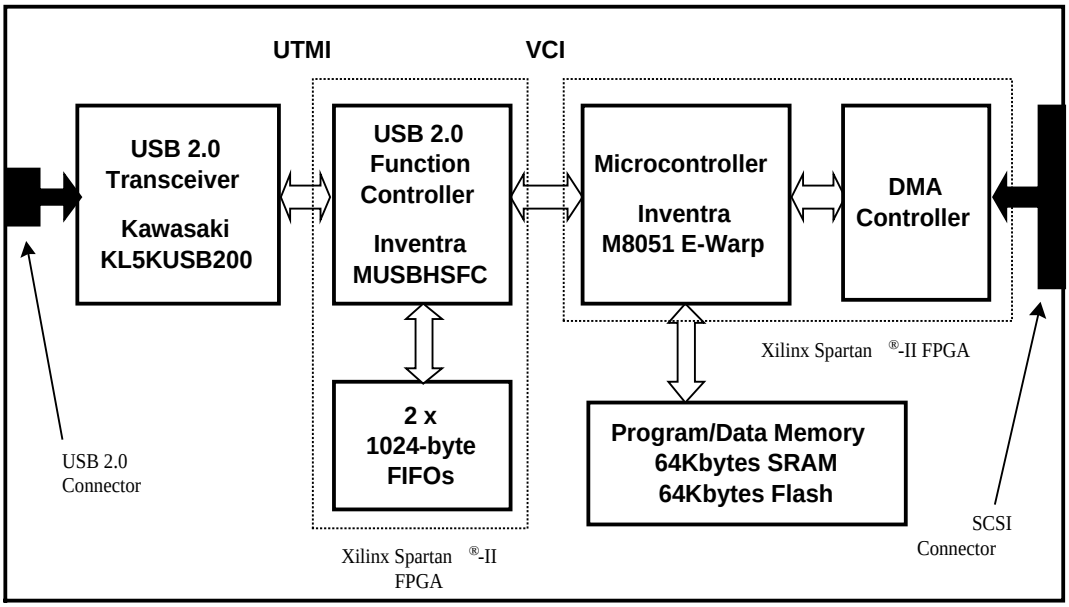
The device code occupies less than 10K of program memory, and uses wide SCSI data transfers. It also uses a DMA controller to transfer data directly between the SCSI interface and the VCI interface to help sustain the high-bandwidth data transfers supported by USB 2.0.

Demonstration Overview

The USB device is demonstrated using a PC, loaded with Windows 2000 Professional, and including an Intel PDK USB 2.0 Host controller PCI card. The SCSI interface of the demo card is interfaced to a commercially-available SCSI disk drive.

The connection between PC and the demo board is made using a standard USB-compliant cable. Connection between the SCSI interface and the disk drive is via a standard SCSI cable.

USB 2.0 Transfer System Block Diagram



The USB 2.0 Function Controller

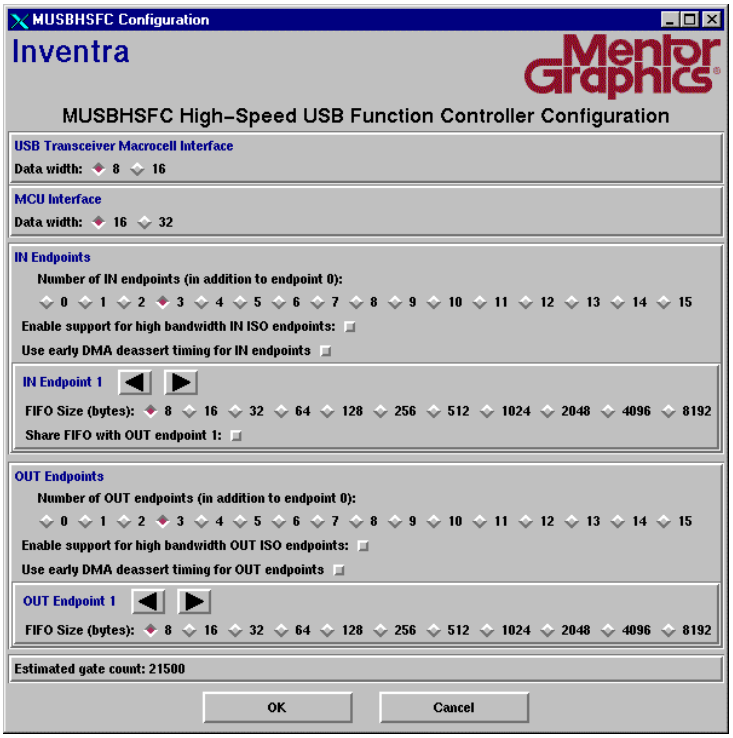
The Mentor Graphics Inventra™ MUSBHSFC

The MUSBHSFC core provides a USB function controller that complies with the USB 2.0 specification for high/full-speed (480/12 Mbits/s) functions.

The core is user-configurable for up to 15 IN endpoints and up to 15 OUT endpoints in addition to Endpoint 0. These additional endpoints can be individually programmed for Bulk/Interrupt or Isochronous transfers.

Each endpoint requires a FIFO to be associated with it. The MUSBHSFC has a RAM interface for connecting to a single block of synchronous single-port RAM which is used for all the endpoint FIFOs. (The RAM block itself needs to be added by the user.)

The size of the FIFO for Endpoint 0 is fixed at 64 bytes and can buffer 1 packet. The MUSBHSFC's FIFO interface is configurable with regard to the other endpoint FIFOs which may be from 8 to 8192 bytes in size and can buffer either 1 or 2 packets. Separate FIFOs may be associated with each endpoint: alternatively an IN endpoint and the OUT endpoint with the same Endpoint number can be configured to use the same FIFO, for example to reduce the size of RAM block needed.



The MUSBHSFC provides a USB 2.0 Transceiver Macrocell Interface (UTMI Specification version 1.04) to connect to an 8/16-bit high/full-speed transceiver. The design also features a 16/32-bit VCI-compatible interface to connect to a processor bus. Access to the FIFOs and the internal control/status registers is via the 16/32-bit VCI-compatible interface. The device also offers DMA access to the Endpoint FIFOs.

The MUSBHSFC provides all the USB packet encoding, decoding, checking and handshaking – interrupting the CPU only when endpoint data has been successfully transferred.

A graphical user interface script is provided for configuring the core to the user's requirements.

8051-Compatible Microcontroller

The Mentor Graphics Inventra™ M8051 E-Warp

The M8051 E-Warp offers a complete, high performance 8051 core and development kit, based around Mentor Graphics' highly successful M8051 Warp implementation of this popular 8-bit microcontroller.

The M8051 E-Warp is the only 8051-compatible soft core to surpass 50Mips performance reliably. It is also the lowest power core available today. Power control mechanisms are built into the state machine, CPU and peripherals.

The M8051 E-Warp is also 100% legacy compatible, preserving the user's investment in industry-standard 8051 tool suites. It does not use instruction set extensions and exotic clocking mechanisms that require expert hand-editing of design tools.

The M8051 E-Warp can be configured to suit a wide range of user requirements. For example, it can be configured to work with either synchronous or asynchronous memory; it can have separate Program and External Data Memory interfaces or a single multiplexed interface; and it can offer either one, two or eight data pointers and two or four levels of interrupt priority. Wait state support is provided for slow memory devices.

Debug Environment

The M8051 E-Warp offers a Debug Mode together with an On-Chip Instrumentation (OCI™) interface. This interface offers a set of dedicated Debug signals, which may be used by external debug hardware to provide a range of debugging facilities.

These facilities are intended to be used in conjunction with the ISA-WARP 8051 In-Target System Analyzer from First Silicon Solutions (FS2).

The OCI™ interface, working in conjunction with in-circuit emulation tools, enables in-situ, at-speed validation of the board application program. The ISA-WARP 8051 In-Target Analyzer provides a PC-based validation platform for the USB2.0 board.

M8051 E-Warp Debugger Kit

The debug interface provides a range of debugging features from basic stop/start or single-step execution and breakpoint support to reconstruction of execution history and capture of data memory, program memory and SFR accesses.

A graphical, source level debugger program supplied with the ISA-WARP 8051 provides an intuitive, easy to use interface. The debugger runs on a PC over high-speed parallel port.

The ISA-WARP 8051 is contained in a compact chassis that connects to the board using a standard 20 pin AMP debug connector. It requires access to just 6 of the M8051 E-Warp's pins.

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